## Logical analysis of firewall configurational correctness

© V.V. Devyatkov, Myo Than Tun

Bauman Moscow State Technical University, Moscow, 105005, Russia.

This article focuses on static analysis for firewall configuration errors. In contrast to the well-known works in this paper we propose to describe the behavior of the firewalls as process models and not as access control lists ACL (ACL – Access Control Lists). The expressive possibilities of process models are much wider and more developed that allow describing a much more complex model of the configuration software. Static analysis is proposed to realize by the methods of logic programming as a proof properties of the configuration process that is much more elegant, full and unfettered approach to validate the configuration of firewalls. Requirements (properties) of correctness is proposed to formalize in the language of modal logic. The formal description of the properties is transformed in the goal of Prolog. The article gives examples of logic programs to validate the configuration of firewalls in Prolog and the results of their tests.

*Keywords:* firewall, process, static analysis of correctness, logic programming language *Prolog.* 

**Deviatkov V.V.** (b. 1939) graduated from the Leningrad Institute of Fine Mechanics and Optics in 1963. Dr. Sci. (Eng.), Professor, Head of the Department Information System and Telecommunication of Bauman Moscow State Technical University, D.Sc(Doctor of Science)(1981), professor. Author of over 120 scientific publications (including 3 monographs). e-mail: deviatkov@bmstu.ru

**Myo Than Tun** (b. 1984) graduated from Lomonosov Moscow State University in 2010. Second year postgraduate student of Computer System and Network Department of Bauman Moscow State Technical University. e-mail: myothanhtun@gmail.com